

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A reconfigurable processor integrated circuit, comprising:

a processor core for operating on a set of instructions to carry out predefined processes;

a plurality of input/output pins;

a plurality of functional input/output blocks associated with said processing core to allow

5 said processing core to interface with said plurality of input/output pins, each of said functional input/output blocks having an associated functionality and a requirement for a defined number of said plurality of input/output pins wherein the total of said defined number for all of said plurality of functional input/output functional blocks exceeds the number of said plurality of input/output pins;

10 a reconfigurable interface for interfacing between said processor core said associated functional blocks and said plurality of input/output pins, said reconfigurable interface operable to define how each of said plurality of input/output pins interfaces with select ones of said plurality of functional blocks ~~associated with said processor core~~ and the associated functionality ~~associated therewith~~ in accordance with configuration information; and

15 a non-volatile memory for storing said configuration information, such that said stored configuration information can be altered.

Claim 2 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1, wherein said plurality of input/output pins are configured in functional groups.

Claim 3 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1, wherein said processor core has a plurality of inputs/outputs and each of said plurality of said input/output pins can be interfaced with any of said plurality functional input/output blocks by said reconfigurable interface.

Claim 4 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1,

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wherein said reconfigurable interface is programmable by said user.

Claim 5 (Previously Presented): The reconfigurable processor integrated circuit of Claim 1, wherein said processor core is a digital processor core and further comprising an analog section for interfacing via input/output analog pins with analog signals and for interfacing with said processor core with a digital interface.

Claim 6 (Previously Presented): The reconfigurable processor integrated circuit of Claim 5, wherein said input/output analog pins are not reconfigurable with said reconfigurable interface.

Claim 7 (Canceled)

Claim 8 (Withdrawn): An integrated circuit, comprising:

a processing core for executing a plurality of instructions to carry out a predefined process;

5 a first memory for containing user defined instructions on which said processing core operates; and

a second imbedded memory for containing proprietary instructions on which said processing core operates and which proprietary instructions are accessible by instructions operating from said first memory, and which second memory is not accessible external to the integrated circuit, said
10 second memory only accessible by instructions in said second memory when executing an instruction therein.

Claim 9 (Withdrawn): The integrated circuit of Claim 8, wherein said first memory is loaded in a first and initializing operation prior to the user programming said second memory and said first memory locked after such loading from access external to the integrated circuit.

Claim 10 (Withdrawn): The integrated circuit of Claim 8, and further comprising a proprietary

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interface to said first and second memory.

Claim 11 (Withdrawn): The integrated circuit of Claim 10, wherein said first and second memories are flash memory.

Claim 12 (Withdrawn): The integrated circuit of Claim 11, wherein said proprietary interface comprises a JTag interface.

Claim 13 (Withdrawn): The integrated circuit of Claim 8, wherein said first memory includes debugging instructions to allow the user to monitor and debug program instructions contained within said second memory, such that the integrated circuit can be operated within its operating environment and debugged therein.

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